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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/826,661	04/05/2001	Yongjun Hu	303.098US4	4539

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NGUYEN, JOSEPH H

ART UNIT	PAPER NUMBER
2815	12

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/826,661	Applicant(s) HU, YONGJUN	
	Examiner Joseph Nguyen	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *49-54 and 71-107* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *49-54 and 71-107* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 48, 50-54, 71-83, 85-96, 98-106 are rejected under 35 U.S.C. 102(e) as being anticipated by Sim.

Regarding claim 48, Sim discloses on **figure 3B** a contact hole for a semiconductor device comprising "a bottom surface of a first material [22]; at least one vertical sidewall of a second material [26]; a generally planar layer of a third material covering only the bottom surface, the third material [32] having a graded stoichiometry between two different elements".

Regarding claim 50, Sim discloses the first material 22 is silicon.

Regarding claim 51, Sim discloses the second material 26 is an insulator.

Regarding claim 52, Sim discloses the planar layer 32 contacts the sidewalls.

Regarding claim 53, Sim discloses the third material 32 is substantially confined to the bottom of the hole.

Regarding claim 54, Sim discloses the third material 32 is a silicide.

Regarding claim 71, Sim discloses on **figure 3B** a semiconductor device having a substrate 22, a contact hole in a layer of insulator material 26 directly overlying the substrate, the hole comprising a bottom surface having at least one generally planar layer of conductive material 32 including at least two different constituent elements; and a vertical sidewall consisting substantially entirely of the aforementioned layer of insulator material 26.

Regarding claim 72, Sim discloses on figure 3B the planar layer 32 contacts the lower end of the sidewall.

Regarding claim 73, Sim discloses on figure 3B the planar layer 32 does not extend substantially up the sidewall from the bottom surface.

Regarding claim 74, Sim discloses on figure 3B the planar layer 32 is an alloy or a composite.

Regarding claim 75, Sim discloses on figure 3B the planar layer is a silicide.

Regarding claim 76, Sim discloses on figure 3B the planar layer 32 includes a refractory metal.

Regarding claim 77, Sim discloses on figure 3B a semiconductor device having a substrate 22, a contact hole in a layer of insulator material 26 directly overlying the substrate, the hole comprising a bottom surface having at least one bottom layer of conductive material 32 including at least two different constituent elements and having a thickness variation less than about 50% and a vertical sidewall consisting substantially entirely of the aforementioned layer of insulator material 26.

Regarding claim 78, Sim discloses on figure 3B the hole has a high aspect ratio.

Regarding claim 79, Sim discloses on figure 3B the aspect ratio is at least 4.

Regarding claim 80, Sim discloses on figure 3B the thickness variation is less than about 20%.

Regarding claim 81, Sim discloses on figure 3B the thickness variation is less than 10%.

Regarding claim 82, Sim discloses on figure 3B a semiconductor device having a substrate 22, a contact hole in a layer of insulator material 26 directly overlying the substrate, the hole comprising a vertical sidewall consisting substantially entirely of the aforementioned layer of insulator 26; and a bottom surface having at least one generally planar bottom layer of conductive material 32 having a graded stoichiometry between two different constituent elements in the bottom layer.

Regarding claim 83, Sim discloses on figure 3B the substrate 22 is silicon and the insulator material is an oxide, a nitride or a glass.

Regarding claim 85, Sim discloses on figure 3B the conductive material 32 includes a silicide of a metal.

Regarding claim 86, Sim discloses on figure 3B the metal is a refractory metal.

Regarding claim 87, Sim discloses on figure 3B a semiconductor device having a substrate 22, a contact hole in a layer of insulator material 26 directly overlying the substrate, the hole comprising a bottom surface having at least one generally planar bottom layer of a conductive material 32 including at least two different constituent elements; and a vertical sidewall comprising the aforementioned layer of insulator material 32 and being free of the conductive elements.

Regarding claim 88, Sim discloses on figure 3B the planar layer contacts the lower end of the sidewall.

Regarding claim 89, Sim discloses on figure 3B the planar layer does not extend substantially up the sidewall from the bottom surface.

Regarding claim 90, Sim discloses on figure 3B the planar layer is an alloy or a composite.

Regarding claim 91, Sim discloses on figure 3B the planar layer includes a silicide.

Regarding claim 92, Sim discloses on figure 3B the planar layer 32 includes a refractory metal.

Regarding claim 93, Sim discloses on figure 3B a semiconductor device having a substrate 22, a contact hole in a layer of insulator material directly overlying the substrate, the hole comprising a bottom surface having at least one generally planar bottom layer of conductive material 32 including a silicide of a metal, a vertical sidewall comprising the aforementioned layer of insulator material 26, and being substantially free of the metal.

Regarding claim 94, Sim discloses on figure 3B the metal is a refractory metal.

Regarding claim 95, Sim discloses on figure 3B the insulator material 26 is an oxide, a nitride or a glass.

Regarding claim 96, Sim discloses on figure 3B the planar layer has a graded stoichiometry.

Regarding claim 98, Sim discloses on figure 3B an integrated circuit comprising a substrate 22; a layer of insulating material 26 overlying the substrate and containing at least one contact hole having only that layer as a sidewall and having a bottom surface contacting the substrate 22; and at least one generally planar layer 32 of conductive layer material including at least two different constituent elements covering the bottom surface of the hole.

Regarding claim 99, Sim discloses on figure 3B the planar layer 32 contacts the lower end of the sidewall.

Regarding claim 100, Sim discloses on figure 3B the planar layer does not extend substantially up the sidewall from the bottom surface.

Regarding claim 101, Sim discloses on figure 3B the planar layer 32 is an alloy or a composite.

Regarding claim 102, Sim discloses on figure 3B the planar layer 32 includes a silicide.

Regarding claim 103, Sim discloses on figure 3B the planar layer 32 includes a refractory metal.

Regarding claim 104, Sim discloses on figure 3B an integrated circuit comprising a substrate 22; a layer of insulating material 26 overlying the substrate 22 and containing at least one contact hole having only that layer as a sidewall and having a bottom surface contacting the substrate; and at least one generally planar layer 32 of conductive material covering the bottom surface, the planar layer including a silicide of a metal, the metal being substantially entirely confined to the bottom surface in the hole.

Regarding claim 105, Sim discloses on figure 3B the planar layer 32 contacts the lower end of the sidewall.

Regarding claim 106, Sim discloses on figure 3B the planar layer 32 has a graded stoichiometry.

Claims 48, 50-54, 71-83, 85-96, 98-106 are rejected under 35 U.S.C. 102(e) as being anticipated by De Bruin.

Regarding claims 48, 50-54, 71-83, 85-96, 98-106, De Bruin discloses on ***figure 4*** all the structures set forth in the claimed invention.

Claims 48, 50-54 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen.

Regarding claim 48, Chen discloses on figure 3B a contact hole for a semiconductor device comprising "a bottom surface of a first material [31]; at least one vertical sidewall of a second material [33]; a generally planar layer of a third material covering only the bottom surface, the third material [36] having a graded stoichiometry (col. 4, lines 7-12) between two different elements".

Regarding claim 50, Chen discloses the first material 31 is silicon.

Regarding claim 51, Chen discloses the second material 33 is an insulator.

Regarding claim 52, Chen discloses the planar layer 36 contacts the sidewalls.

Regarding claim 53, Chen discloses the third material 36 is substantially confined to the bottom of the hole.

Regarding claim 54, Chen discloses the third material 36 is a silicide.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen as applied to claim 48 above, and further in view of Miyamoto.

Regarding claim 49, Chen discloses substantially all the structure set forth in the claimed invention except the hole having a high aspect ratio. However, Miyamoto discloses on figure 3 the hole having a high aspect ratio (col. 9, lines 3-8). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Miyamoto by having the hole having a high aspect ratio for the purpose of providing a good coverage over a surface of the silicon substrate.

Claims 84, 97,107 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sim as applied to claims 82, 96 and 106 above, and further in view of Chen.

Regarding claims 84, 97 and 107, Sim discloses substantially all the structures set forth in the claimed invention except the planar layer comprising multiple layers having mutually different stoichiometry. However, Chen discloses on figure 3B the planar layer 36 comprising multiple layers having mutually different stoichiometry. In

view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Sim by having the planar layer comprising multiple layers having mutually different stoichiometry for the purpose of improving the electrical interconnects within a semiconductor device.

Response to Arguments

Applicant's arguments filed on 9/30/2002 have been fully considered but they are not persuasive.

With respect to claims 48-54, applicant argues that Chen does not disclose such grading in the bottom layer as recited in claim 48. However, Chen clearly discloses on figure 3B a generally planar layer of a third material 34, 36 covering only the bottom surface, the third material 34, 36 having a graded stoichiometry between two different elements (col. 4, lines 8-15). Therefore, Chen reference still reads on claims 48-54 herein.

Applicant's arguments with respect to claims 71-107 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (703) 308-1269. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for

the organization where this application or proceeding is assigned is (703) 308-7382 for regular communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JN
November 1, 2002

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800